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10/603,217	06/24/2003	Eric E. Edwards	X-1330 US	4304

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EXAMINER	
ENGLUND, TERRY LEE	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 08/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/603,217	EDWARDS, ERIC E.	
	Examiner	Art Unit	
	Terry L Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11, and 14-18* is/are rejected.

7)☒ Claim(s) *12 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities: Page 5, paragraph 0028, line 2 "402" is believed to refer to --420-- since that resistor (shown in Fig. 6) actually corresponds to Fig. 1's resistor "112". Page 6, paragraph 031, line 5 "322-1 to 322-M1" should be --324-1 to 324-M1-- to correspond to the diode-connected transistors related to node B. Appropriate corrections are required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 8, 10-11, and 14-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Frisch et al. (Frisch). Fig. 4 shows power up reset circuit 20 comprising comparator 38; first/second inputs -/+; output 41; diode connected transistor 24 and resistor 26 coupled to first input –; power supply voltage Vdd; resistor 32 and diode connected transistor 34 coupled to second output +; and ground Vss. These elements correspond to power up reset circuit 100 comprising comparator 102; first/second inputs -/+; output 116; diode connected transistor 110 and resistor 114 coupled to first input –; power supply voltage Vdd; resistor 112 and diode connected transistor 108 coupled to second output +, and ground (unlabeled) shown in the applicant's own Fig. 1, with only one minor exception. Frisch's diode connected transistor 34 is a PMOS transistor, wherein the applicant's corresponding diode connected transistor 108 is an

NMOS transistor. Therefore, details of the actual structure and operation are not necessary, and one of ordinary skill in the art would understand that claims 1-3, 8, 10-11, and 14-15 are anticipated.

Claims 1-4, 8, 10-11, and 14-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Guritz. Fig. 9 shows power up reset circuit 10 comprising comparator 14 with first/second inputs coupled to their respective circuits 18,20. Figs. 3a, 4a-4c, 5a, and 5b each show an example of what each circuit might comprise, wherein any combination can be used as long as voltage V1,V2 will have a selected cross over point (e.g. see Figs. 6-8, and column 4, lines 28-40). On lines 35-36 of column 3, Guritz discloses the load circuit (e.g. shown in Figs. 4a-4b and 5a-5b), can be a resistor. Assuming each load is a resistor, when circuits 18 and 20 utilize the respective circuits shown in Figs. 4a and 5b, the power up reset circuit corresponds to the applicant's own Fig. 1; and when circuits 18 and 20 utilize the respective circuits shown in Figs. 3a and 5b, the power up reset circuit then corresponds to the applicant's own Fig. 3. Therefore, details of the actual structure and operation are not necessary, and one of ordinary skill in the art would understand that claims 1-3, 8, 10-11, and 14-15 are anticipated. When Fig. 4c is used as the circuit coupled to the first input of the comparator, it comprises a first plurality of diode connected transistors T5,T6, and claim 4 is anticipated.

Claims 1-3, 6, and 14-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Chevallier et al. (Chevallier). Fig. 2 shows a power up reset circuit in Fig 2 comprising comparator 12 with its first/second inputs coupled to resistor 24,diode connected transistor 21 and 16 (one type of a resistor divider), respectively. As shown in Fig. 3A, reset signal COMPARATOR OUTPUT is generated when the first/second inputs REFERENCE OUTPUT/

TRANSLATOR OUTPUT are approximately the same, thus anticipating claim 1. Due to the configuration of 14 and 16, first input 15 (i.e. REFRENCE OUTPUT) is maintained at a one or more threshold voltage difference with respect to power supply voltage Vcc, and the resistor divider type configuration maintains second input (i.e. TRANSLATOR OUTPUT) at a one or more threshold voltage difference from ground potential, anticipating claims 2-3. [To better visualize those voltage differences, see Fig. 3A.] Transistor 28 is used as a hysteresis circuit, which one of ordinary skill in the art would understand protects the power up reset circuit from glitches (e.g. see column 6, lines 1-7), anticipating claim 6. Interpreting Figs. 2-3 in a slightly different manner, power supply voltage Vcc increases to a predetermined level; 16 causes first input TRANSLATOR OUTPUT to increase in voltage to at least one diode threshold voltage above ground; 14 causes second input REFERENCE OUTPUT to increase in voltage to at least one diode threshold voltage below power supply voltage Vcc; and when the first/second inputs are approximately the same, comparator 12 generates power up reset signal COMPARATOR OUTPUT. Since the output transitions a high logic level to a low logic level (e.g. see Fig. 3a), claims 14-15 are anticipated. Once the power up reset signal has been generated, transistor 28 will be turned on via 43, thus changing the voltage trip point of the power up reset circuit, and claim 16 is anticipated. It is understood that an unasserted enable signal /ENABLE will prevent the comparator from consuming any static current during low power mode operations (e.g. see column 4, lines 1-4). Therefore, claim 17 is also anticipated.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4-7, 9, and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Frisch in view of their own respective independent claim 1, 8, and 14 described above. The Frisch reference does not clearly show or disclose: 1) a plurality of diode connected transistors; 2) a hysteresis circuit; 3) a Field Programmable Gate Array (FPGA); 4) changing a voltage trip point; 4) unasserting an enable signal; or 5) a Programmable Logic Device (PLD). It would have been obvious to one of ordinary skill in the art to replace each of the single diode connected transistors (24 and 34) of Frisch with a corresponding plurality of diode connected transistors coupled in series, thus rendering claims 4 and 5 obvious. By changing the number of diode connected transistors, one of ordinary skill in the art can determine how many threshold drops (below Vdd or above Vss) are required to set the desired trip point of the circuit. It would have been obvious to one of ordinary skill in the art to couple a hysteresis type circuit to the comparator to protect the circuit from glitches, rendering obvious claims 6 and 7. A hysteresis circuit would allow the circuit to provide a reset signal once the power supply voltage reaches a minimum level, and then reduce the initial voltage level of the circuit's triggering point to minimize the possibility a glitch (e.g. a small, temporary drop in power supply voltage) will inadvertently re-trigger the reset signal. Without the hysteresis circuit, a glitch could cause the system to interrupt its normal operation, wherein the power-up related sequence would restart again. With the addition of the hysteresis circuit to Frisch's circuit, the voltage trip point of the circuit is changed as described above, thus rendering claim 16 obvious. It would have been obvious to one of ordinary skill in the art to use Frisch's power up reset circuit with a Field

Programmable Gate Array (FPGA), and/or Programmable Logic Device (PLD). Therefore, claims 9 and 18 are rendered obvious. It is desirable to ensure FPGA and PLD related circuits begin their normal operations only after the power supply voltage has reached at least their minimal, predetermined operating level. Otherwise, if they start operation when powered by a voltage below that level, they may operate inefficiently, or even cause corruption of data they are associated with. It also would have been obvious to one of ordinary skill in the art to utilize an enable signal with the comparator, wherein the comparator would only be used when the power up sequence is required. Under normal operation (e.g. after the desired power supply voltage has been reached), the comparator could be disabled to minimize power, and also reduce or prevent any static current flow within the circuit, thus rendering claim 17 obvious. Low power consumption, and minimal static current, will allow the overall system to operate longer (e.g. if the system is being run on batteries), and help reduce the amount of heat generated by any unnecessary current flow.

Claims 5-7, 9, and 16-18 are also rejected under 35 U.S.C. 103(a) as being unpatentable over Guritz in view of their own respective independent claim 1, 8, and 14 described above. Similar to the Frisch reference described above, the Guritz reference does not clearly show or disclose: 1) a second plurality of diode connected transistors; 2) a hysteresis circuit; 3) a Field Programmable Gate Array (FPGA); 4) changing a voltage trip point; 5) unasserting an enable signal; or 4) a Programmable Logic Device (PLD). Applying the same type of reasoning as applied to the Frisch reference above, claims 5-7, 9, and 16-18 are rendered obvious with respect to the Guritz circuit.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chevallier et al. (Chevallier) as applied to claim 14 above. As previously described, Chevallier shows/discloses a circuit/method for generating a power up reset signal. However, the reference does not clearly show or disclose its relationship to a Programmable Logic Device. It would have been obvious to one of ordinary skill in the art to use Chevallier's circuit with a PLD, thus rendering obvious claim 18. This would allow the PLD to be activated only after the power supply voltage has reached a minimal, predetermined voltage level, thus minimizing inefficient operation and/or possible corruption of data.

No claim is allowable as presently written.

Allowable Subject Matter

However, claims 12-13 are only objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. There is presently no strong motivation to modify or combine any prior art reference(s) to ensure: 1) the reset signal at the output node is coupled to the first/second capacitors as recited within claim 12; and 2) the hysteresis circuit comprises a feedback transistor and third resistor coupled in parallel, with the third resistor connected to the first diode connected transistor as recited within claim 13.

Prior Art

The other prior art references cited on the accompanying PTO-892 are deemed relevant to at least some of the claimed limitations. Although not used in any formal rejections described above, Fig. 7 of Kwon is of special interest. It shows comparator 300 with its first/second inputs coupled respectively to circuits 200/100, wherein each one of those circuits comprises at least

one resistor coupled in series with at least one diode connected transistor (e.g. see 202,203 of 200, and 103,104 of 100). Therefore, this circuit reads on the basic structure and/or limitations recited in at least claims 1-3, 14 and 17. The circuit also shows means 205,101,SW2,SW1 for disabling the circuit, and preventing any unnecessary current from flowing. Maccarrone et al.'s Fig. 2 shows the two inputs +/- of comparator 2 coupled to respective circuits 11 and 12. Circuit 11, shown in Fig. 3, has diode connected transistor G4 coupled directly to Y (provided to input + of the comparator), and Fig. 4 shows circuit 12 having a resistor divider R1,R2 coupled directly to G (provided to input – of the comparator). Therefore, this reference also reads on the basic structure and/or limitations recited in at least claims 1-3. The reference of Maccarrone et al. also shows: 1) enable signal EN for enabling/disabling comparator 2, as well as circuits 11 and 12, when required; and 2) the use of first capacitor C coupled between reset signal INTPOR and power supply vdd (but does not show a second capacitor coupled between INTPOR and ground). Therefore, these references should be carefully reviewed and considered.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund

27 July 2004

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